Compact modeling of metal-insulator-graphene (MIG) interfacial memristor for parallel programming in 1R crossbar array

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Conventionally, a 1R crossbar array is programmed in a column-wise or a cell-wise fashion [1]. Recent advancements in programming scheme, circuit design, and device engineering have explored the feasibility of complete parallel programming a memristive crossbar array with time complexity of *O(1)* [2, 3]. This scheme is promising to accelerate deep neural network (DNN) training based on stochastic gradient descent, as the training speed becomes independent of the number of neurons in each layer. However, implementing a fully functional chip based on this update scheme requires cross-hierarchical co-design, and accurate physics-based compact modeling is essential to this goal.

In this work, we demonstrate that metal-insulator-graphene (MIG) interfacial memristor is proved to enable parallel programming. We develop a compact model based on experimental I-V relationship that enables the prediction of I-V relationship and conduction tuning behavior. The experimental I-V characteristics were measured on a 20 μm by 20 μm device from 0 to 2.5V double sweep, where each sweep lasts for 10s. The voltage on the device is thus swept for 8 times to potentiate the device fully. The voltage on the device is then swept from 0 to -2.5V back and forth, with the same sweep speed for 8 times to fully depress the device. The measured I-V was separated into 4 segments then transformed into different forms of relationship to extract parameters for possible conduction and switching mechanisms, including ohmic/space-charged-limited conduction (SCLC), Poole-Frenkel (PF) emission, direct tunneling and Fowler-Nordheim (FN) tunneling [4]. The evolution of parameters with time was then extracted for each mechanism, and a function is proposed to fit each evolution. State function x and its change with time dx/dt were introduced to depict the change of the conductance of MIG interfacial memristor. The completed model takes an arbitrary voltage-time relationship $V(t)$ as an input and is able to produce similar I-V relationship and conductance tuning characteristics including parallel programming scheme as measured experimentally. This model can be directly integrated into circuit design software, enabling device-circuit co-design to realize a functional macro of fully parallel programming for DNN training acceleration.

References

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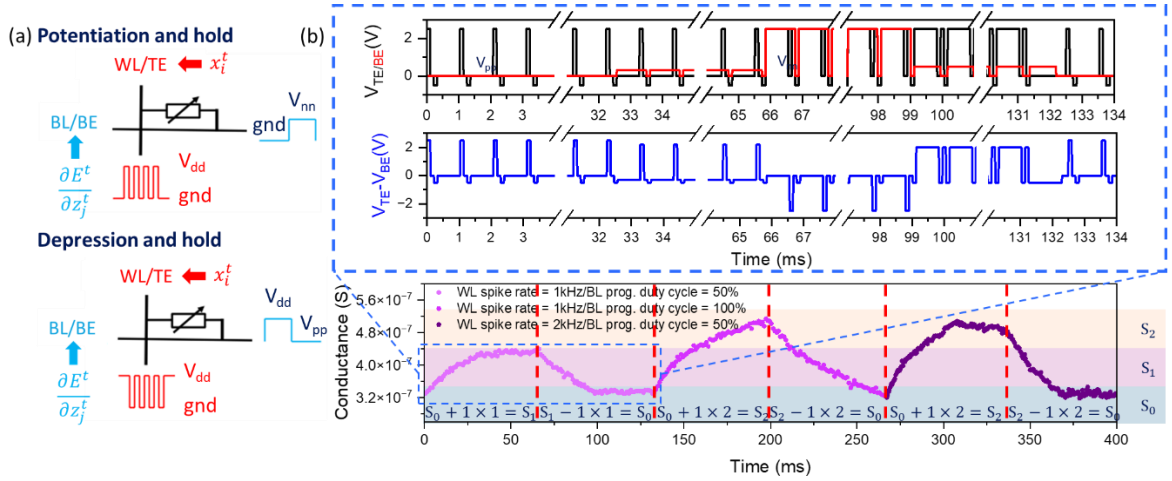

Fig. 1 (a) Proposed programming scheme for fully-parallel weight update based on stochastic gradient descent. **(b)** Experimental waveform and conductance tunning curve inside the 1R MIG passive array.

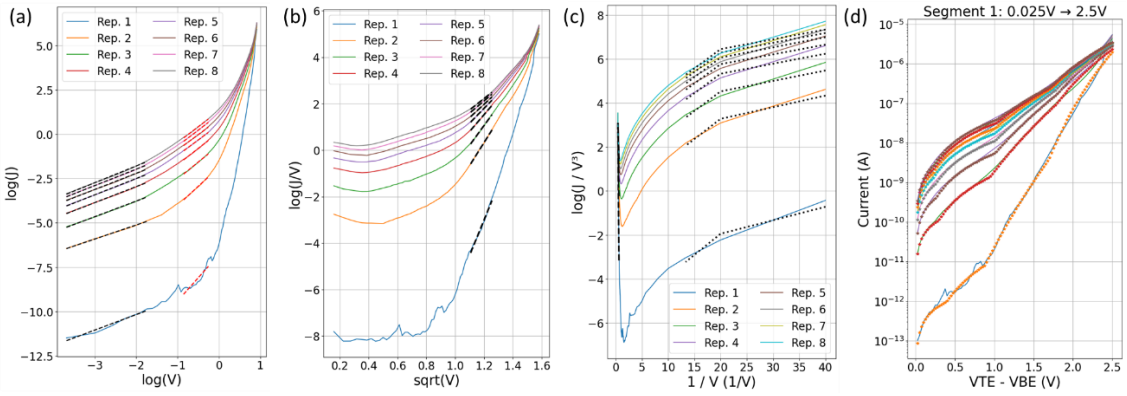

Fig. 2 (a) Extraction for Ohmic conduction and SCLC for segment 1, i.e., 0.025V to 2.5V. **(b)** Extraction for PF emission. **(c)** Extraction for direct and FN tunneling. **(d)** Merged IV from the fitted parameters against experimental IV to ensure high accuracy of the fitting.

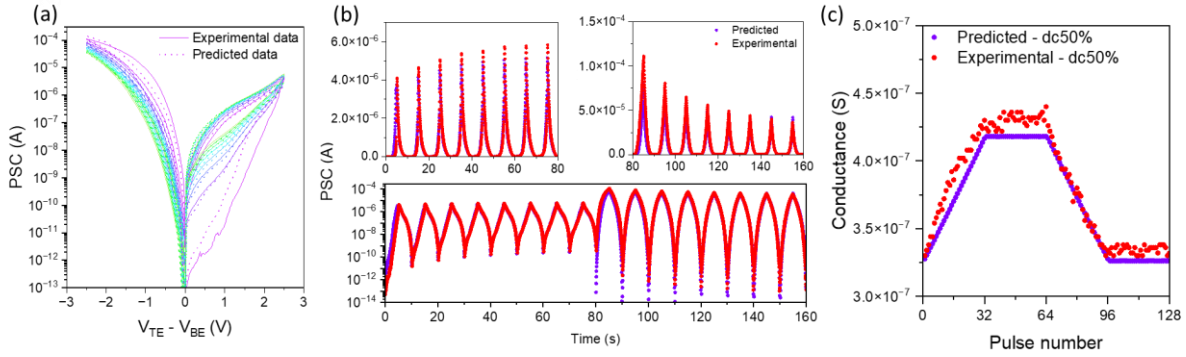

Fig. 3 (a) Predicted I-V relationship in dash line of 8 sweeps from the compact model vs. the experimental I-V relationship. **(b)** I-t relationship in linear and log scale. **(c)** Conductance tunning curve from the compact model vs. the experimental data.